REMARKS/ARGUMENTS

Claims 1-28 remain in the application. Claims 1, 7, 12, 19, and 24 have been amended.

Claim Rejections under 35 U.S.C. § 112, Second Paragraph

Claims 1-28 were rejected under 35 U.S.C. § 112, second paragraph as failing to distinctly claim the invention. In particular, the Office Action points to each of the independent claims and states that the nature of steering is not clear in that there is no recitation of any path variation. Claims 1, 7, 12, 19, and 24 have been amended to make the nature of the steering more clear. Reconsideration and withdrawal of the rejection of claims 1-28 under 35 U.S.C. § 112, second paragraph is respectfully requested.

Claim Rejections under 35 U.S.C. § 102

Claims 1-28 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,442,760 to Rustad et al. ("Rustad").

As amended in response to the § 112, second paragraph rejection, the independent claims recite the steering of a set of instructions into an instruction cache so as to store them in the cache at a location in said instruction cache based on the execution unit or cluster that the instruction requires. Then each of the set of instructions is issued from the instruction cache to a particular one of the execution units. Looking at Fig. 2, for example, instructions are steered and stored into bins of the instruction cache where each bin is assigned to a particular execution unit. As an example, an instruction requiring execution by a floating point execution unit would be steered and stored in the instruction cache (e.g., into a particular bin) based on the floating point execution unit that is required for the instruction's execution.

Rustad concerns instruction folding, where the instructions are located at separate addresses in main memory and/or in a secondary cache. Once a cache miss occurs, an instruction is fetched from a secondary cache or main memory, decoded, and "routed to an appropriate portion of the cache line which controls the execution unit needed to perform that particular instruction." When there is a cache hit, all instructions in the cache line are executed in parallel. Accordingly, Rustad is concerned with what steps to take once a cache miss occurs.

With respect to claims 1-6, this set of claims refers to the decoding of a set of instructions and storing them into an instruction cache based which execution unit is to execute each one of the set of instructions. Rustad refers to the actions taken when a cache miss occurs (note that Claim 6 specifically refers to the situation where a cache miss occurs after the initial steering recited in the prior claims). With respect to claims 7-11, in addition to the above, there is no disclosure in Rustad of scheduling the set of instructions to avoid pipeline stalls and steering thme into the instruction cache based on which execution unit is to execute each one of the set of instructions as recited in these claims. The arguments with respect to claims 1-6 apply to claims 12-18 as well. Claims 19-23 and 24-8 refer to processor architecture that is similar to the components recited in claims 1-18. Accordingly, a feature of the claimed invention, namely the methods and apparatus for handling a set of instructions is not taught by the Rustad reference.

In view of the above, reconsideration and withdrawal of the rejection of claims 1-28 under 35 U.S.C. § 102(b) respectfully requested.

For all the above reasons, the Applicant respectfully submits that this application is in condition for allowance. A Notice of Allowance is earnestly solicited.

The Examiner is invited to contact the undersigned at (202) 220-4255 to discuss any matter concerning this application. The Office is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. § 1.16 or § 1.17 to Deposit Account No. 11-0600.

Respectfully submitted,
KENYON & KENYON

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